REMARKS

Claims 1-10 are pending in this application. Claims 1-6 stand rejected under 35 U.S.C. § 102(b), and claims 7-10 stand rejected under 35 U.S.C. § 103(a). The Applicant has amended claims 1 and 6 to more particularly point out and claim one aspect of the invention. In view of the foregoing amendments, the Applicant respectfully submits that the remaining claims are now in condition for allowance.

In the Drawings

The Examiner objected to Figures 1-3 and requested that the Applicant submit replacement figures bearing a legend such as --Prior Art--. Enclosed herewith are replacement sheets in accordance with the Examiner's request.

In the Claims

Claim Rejections – 35 U.S.C. § 102(b)

Pending claims 1-6 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Apel (U.S. Patent No. 6,894,561). Apel discloses a dual-stage power amplifier controlled by periphery switching. (Abstract, figs. 2-4, 6, and 7.) The power amplifier includes a bias circuit (211). (Col. 3, lines 33-59; fig. 4.) According to Apel, a bias voltage (V_{BIAS1}) is connected to the base terminal of transistor (426) via a resistor (434). (Col. 3, lines 44-56; fig. 4.)

By contrast, according to one aspect of the Applicant's invention, a reference voltage (V_{ref}) is coupled directly to the base terminal of the first transistor. (Para. 27; fig. 4.) According to this aspect of the invention, the reference voltage is made to provide a DC current directly to the base of the first transistor (410), rather than through

a resistor, to avoid any variations in DC bias voltage for the third transistor (430) and related linearity problems. (Para. 26-27; fig. 4.)

The Applicant has amended independent claims 1 and 6 to more particularly point out and claim this aspect of the invention. As a result of the amendment to claim 1, claims 1-5 all now require "a first transistor with a reference voltage coupled directly to its base terminal." Similarly, as amended, claim 6 recites "coupling a reference terminal directly to a base terminal of a first transistor." Apel does not show, describe, or suggest these features of claims 1-6. To the contrary, Apel teaches away from this aspect of the invention by showing and describing a resistor (434) connected between the reference voltage (VBIAS1) and the transistor (426). (Col. 3, lines 44-56; fig. 4.) Accordingly, the Applicant respectfully requests that the Examiner withdraw these rejections under 35 U.S.C. § 102(b) with respect to independent claims 1 and 6, as well as dependent claims 2-5.

Claim Rejections – 35 U.S.C. § 103(a)

Pending claims 7 and 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Apel in view of Nishimura (U.S. Patent No. 6,809,592). As noted above, the Applicant has amended independent claim 6 to more particularly point out and claim one aspect of the invention. As a result of the amendment to claim 6, dependent claims 7 and 8 now require "coupling a reference terminal directly to a base terminal of a first transistor." Neither Apel nor Nishimura shows, describes, or suggests this feature of claims 7 and 8. To the contrary, as noted above, Apel teaches away from this aspect of the invention by showing and describing a resistor (434) connected between the reference voltage (V_{BIAS1}) and the transistor (426). (Col. 3, lines 44-56; fig.

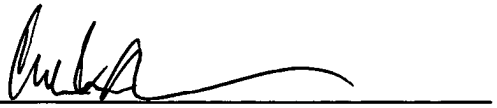
4.) Accordingly, the Applicant respectfully requests that the Examiner withdraw these rejections under 35 U.S.C. § 103(a) with respect to claims 7 and 8.

Pending claims 9 and 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's admitted prior art in view of Apel. Applicant respectfully traverses these rejections. Claims 9 and 10 both require "a power amplifier array coupled to the at least one control circuit," and "an adder coupled to at least one output of the power amplifier array and coupled to an output terminal," wherein "the power amplifier array further comprises at least one bias circuit, said bias circuit including a first transistor with a reference voltage coupled directly to its base terminal." By contrast, as the Examiner has acknowledged, the conventional power amplifier circuit (100) described in the background section of the application does not show, describe, or suggest the bias circuit required by claims 9 and 10. Apel, on the other hand, teaches a bias circuit for use in a dual-stage power amplifier. (Abstract, figs. 2-4, 6, and 7.) Apel does not show, describe, or suggest using the bias circuit with a conventional power amplifier array circuit, including a power amplifier array and an adder coupled to at least one output of the power amplifier array. Nothing in Apel or the background section of the application suggests using the bias circuit of Apel with the conventional power amplifier array circuit. Accordingly, the Applicant respectfully requests that the Examiner withdraw these rejections under 35 U.S.C. § 103(a) with respect to claims 9 and 10.

SUMMARY

Pending claims 1-10, as amended, are allowable. The Applicant respectfully requests that the Examiner grant early allowance of these claims. The Examiner is invited to contact the undersigned attorneys for the Applicants via telephone if such communication would expedite this application.

Respectfully submitted,



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